**Run 1: Login to the Linux account and invoke cadence virtuoso**

**Important notes:**

1. After you finish the simulations, always close the Virtuoso and all other cadence windows properly.
2. Also close the terminal from where you typed **virtuoso &**.
3. After that always logout from your account properly by clicking your username and then logout in top-right corner of the main screen.

**NEVER SHUTDOWN THE PC ONLY LOGOUT FROM TOP RIGHT CORNER**

**Q:** Are you successfully able to login to CentOS and cadence Virtuoso Window is invoked?

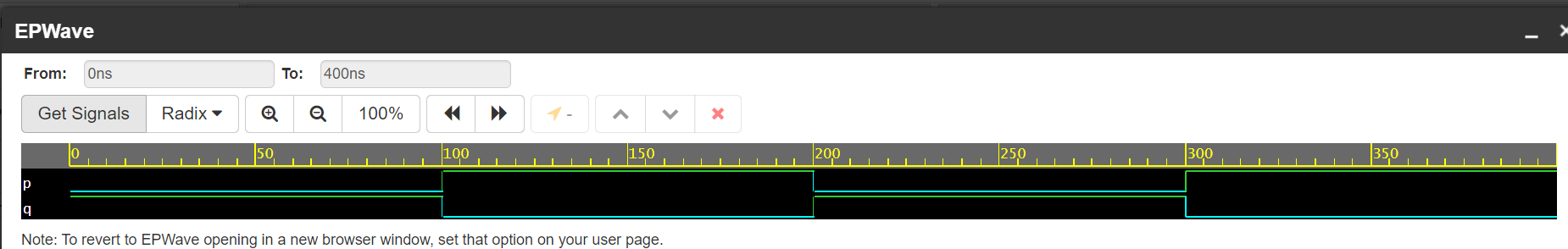
**A:**

**Run 2: Define logic gates and see the propagation delay**

1. **Write verilog code and testbench for NOT gate using gate level modeling and see the waveforms.**

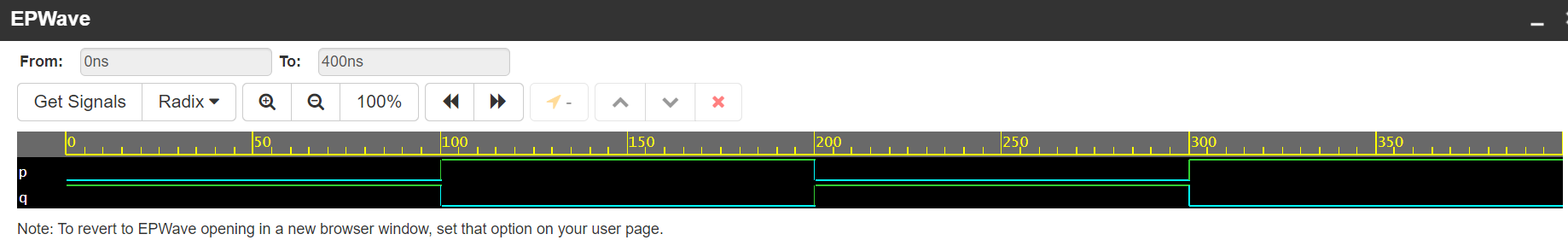
**Q:** Paste the Image of your **Simvision** window where you get the waveforms for the above code.

**A:** [**https://www.edaplayground.com/x/PpGp**](https://www.edaplayground.com/x/PpGp)

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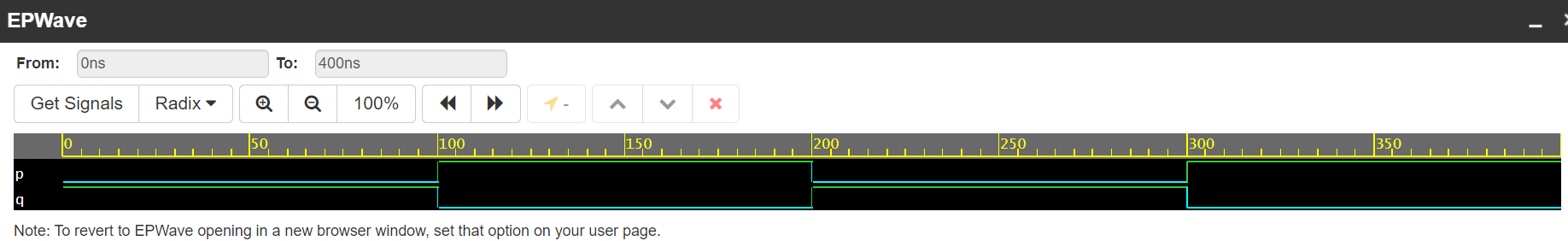
1. **Write the verilog code and testbench for NOT gate using data flow modeling and see the waveforms.**

**Q:** Paste the Image of your **Simvision** window where you get the waveforms for the above code.

**A: https://www.edaplayground.com/x/jFJh**

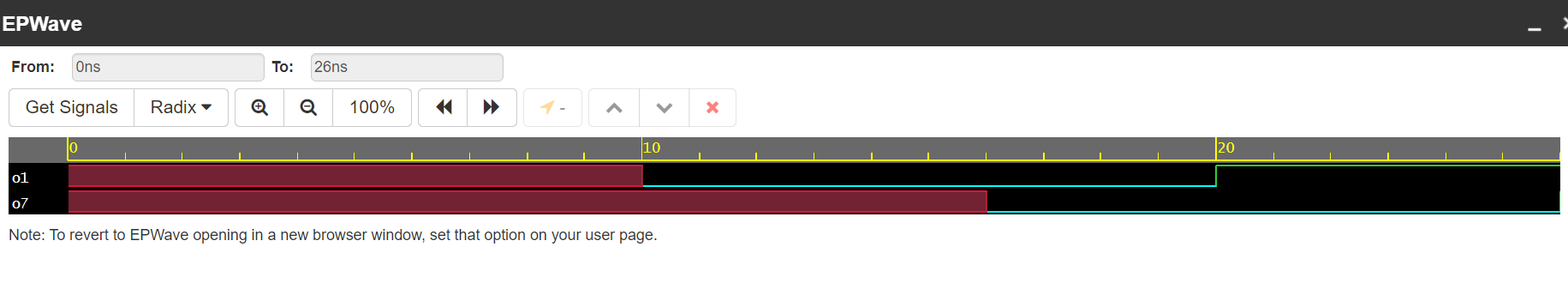
1. **Write the Verilog code and testbench for NOT gate using behavioral modeling and see the waveforms.**

**Q:** Paste the Image of your **Simvision** window where you get the waveforms for the above code.

**A: https://www.edaplayground.com/x/pmrY**

1. **Use any one of the above verilog code of NOT gate as a block and create a series of six NOT gates using structural modeling and see the output with and without delay by applying square wave at the input of first NOT gate.**

**Q:** Paste the Image of your **Simvision** window where you get the waveforms for the above code.

**A:** https://www.edaplayground.com/x/Yf3j

**Run 3: Define logic gates using data flow, gate level modeling and behavioral modeling on** [**www.edaplayground.com**](http://www.edaplayground.com)

**Q:** Note down the setting on the setting left side panel of the website for Simulation.

**A:**  **Testbench + Design:**

**UVM/OVM:**

**Other Libraries:**

* + **Enable TL-Verilog**
  + **Enable Easier UVM**
  + **Enable VUnit**

**Tools & Simulators:**

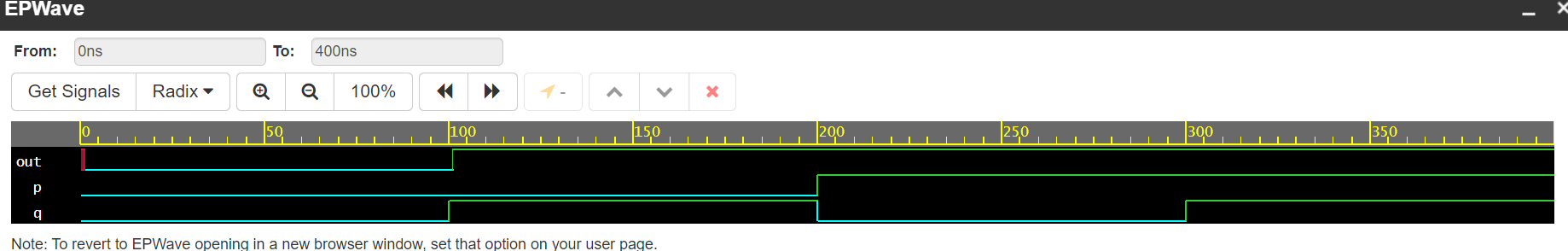
**Compile Run Options:**

**Run Options:**

* + **Use run.do Tcl file**
  + **Open EPWave after run**
  + **Download files after run**

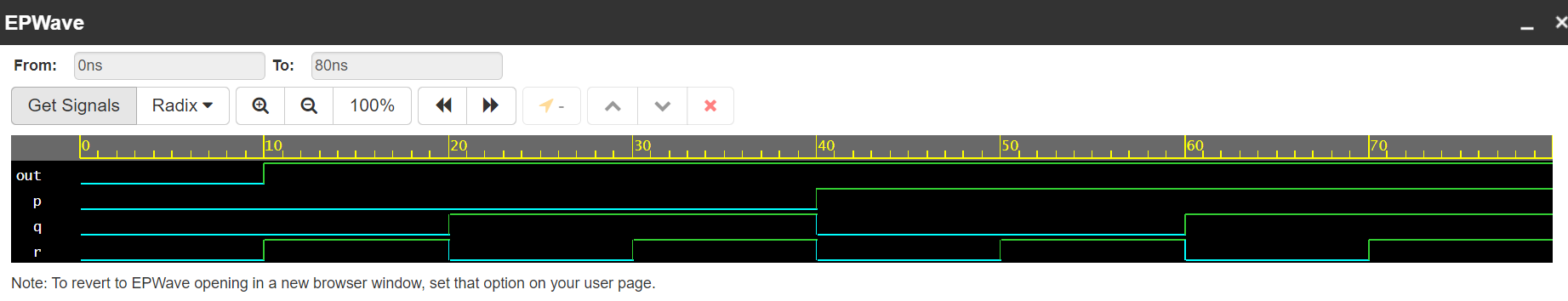
1. **Verilog code and testbench for 2 input OR gate using gate level, data flow and behavioral modeling in one code.**

**Q:** Paste the Image of your **EPWave** window where you get the waveforms for the above code.

**A:** **https://www.edaplayground.com/x/fjFC**

1. **Verilog code and testbench for 3 input OR gate using structural modeling using two 2-input OR gates.**

**Q:** Paste the Image of your **EPWave** window where you get the waveforms for the above code.

**A:** **https://www.edaplayground.com/x/hMaM**